**I CLAIM**

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1. A method for transmitting a continuous digital signal of an arbitrary rate R1 over a synchronous network as a transparent tributary, comprising:

selecting a fixed length container signal of a rate R, where R is higher than said arbitrary rate R1 of said continuous signal; and

at a transmit site, distributing the bits of said continuous signal into valid timeslots of a frame of said container signal and providing stuff bits into invalid timeslots,

wherein said invalid timeslots are uniformly interspersed across said frame.

2. A method as claimed in claim 1, wherein said container signal is a SONET/SDH signal, and said synchronous network is a SONET/SDH network.

3. A method as claimed in claim 2, wherein said SONET/SDH signal further comprises a synchronous tributary.

4. A method as claimed in claim 2, wherein said SONET/SDH signal comprises a plurality of transparent tributaries.

5. A method as claimed in claim 1, wherein said invalid timeslots comprise one of a fixed stuff and an adaptive stuff bit.

6. A method as claimed in claim 5, wherein said step of distributing comprises:

receiving a continuous stream of data bits and determining the phase difference between said arbitrary rate R1 and said rate R;

adding to said continuous stream a definite number of timeslots for accommodating said fixed stuff bits within said frame, and an adjustable number of timeslots for accommodating said adaptive stuff bits within said frame, based on said phase difference.

7. A method as claimed in claim 6, wherein said adjustable number is substantially larger than said definite number.

8. A method as claimed in claim 6, wherein said definite number includes transport overhead TOH timeslots and reminder fixed stuff bits timeslots.

9. A method as claimed in claim 8, further comprising providing maintenance, operation, administration and provisioning information in said TOH timeslots.

10. A method as claimed in claim 6, wherein said step of adding comprises:

partitioning said frame into a number of equally sized data blocks and said definite number of timeslots;

for each block,

determining the number of fixed stuff bits and evenly distributing said fixed stuff bits within said block;

determining a control function $\beta$ indicative of said adjustable number; and

evenly mapping said fixed stuff bits and said adaptive stuff bits uniformly within a next block based on said control function.

11. A method as claimed in claim 10, wherein said step of mapping comprises:

providing a counter C for identifying a timeslot in said block;

defining the binary bit reversal $\alpha$ of said control function $\beta$;

calculating the bitwise transition delta of said counter C; and

determining if a timeslot identified by said counter C is an invalid timeslot, whenever a function Valid $(C,\beta)$ is false; and

providing an adaptive stuff bit into said invalid timeslot.

12. A method as claimed in claim 1, further comprising recovering said continuous signal from said synchronous signal at a receive site, by extracting the data bits of said continuous signal from said valid timeslots of said frame.

13. A synchronizer for mapping a continuous format signal of an arbitrary rate for transport over a synchronous network as a transparent tributary signal, comprising:

a data recovery unit for receiving said continuous format signal and recovering a stream of data bits and a data clock indicative of said arbitrary rate;

a receiver buffer unit for receiving said stream of data bits, determining a phase difference between said arbitrary rate and the rate of a frame of said tributary, and generating a control function β;

a mapping unit for extracting said stream of data bits from said receiver buffer unit at a mapping clock rate, and uniformly distributing a count of stuff bits and data bits into said frame at a block clock rate according to said control function β.

14. A synchronizer as claimed in claim 13, wherein said receiver buffer unit comprises:

an elastic store for temporarily storing an amount of data bits of said stream at said data clock and providing said data bits to said mapping unit at said block clock rate;

a digital PLL for determining the phase difference between said arbitrary rate and said mapping clock and providing said control function β.

15. A synchronizer as claimed in claim 13, wherein said data recovery unit comprises a frequency agile PLL for detecting said arbitrary rate, and a receiver for detecting said data bits using said data clock.

16. A synchronizer as claimed in claim 13, wherein said mapping unit comprises:

a block clock gapper for receiving a clock indicative of the rate of said synchronous frame and providing said block clock of a block rate accounting for all timeslots of said synchronous frame and with gapps accounting for a definite number of timeslots for accommodating fixed stuff bits;

a mapping clock gapper for receiving said block clock and said control signal β and providing a mapping clock of a mapping rate accounting for all timeslots of said synchronous frame and with gapps

accounting for an adjustable number of timeslots for accommodating adaptive stuff bits within said frame; and

a mapper for receiving said block clock and said mapping clock and accordingly mapping said stream of data bits in said frame.

17. A synchronizer as claimed in claim 13, further comprising a receiver OH FIFO for re-arranging a plurality of transport overhead TOH timeslots for seamless transport of said frame within said synchronous network.

18. A synchronizer as claimed in claim 17, further comprising an overhead multiplexer for adding operation, administration, maintenance and provisioning data into said TOH timeslots.

19. A de-synchronizer for reverse mapping a continuous format signal of an arbitrary rate received over a synchronous network as a transparent tributary signal, comprising;

a reverse mapping unit for receiving a frame of said tributary at a block clock rate and a control function $\beta$, and extracting a stream of data bits at a mapping clock rate, while excluding stuff bits according to said control function $\beta$;

a transmitter buffer unit for receiving said data bits, and determining a phase difference between said arbitrary rate and the rate of said frame; and

a data transmit unit for receiving said data bits and transmitting said continuous format signal at a data rate controlled by said phase difference.

20. A de-synchronizer as claimed in claim 19, wherein said control function $\beta$ is received in said frame.